

FileViewEditToolsWindowHelp

Pending

Active

Failed

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L1: (5750) tunnel\$4 adj (barrier layer insul\$6 dielectric)

L2: (14585) (float\$3 adj gate) same (control adj gate)

L3: (1258) 1 same 2

L4: (2222) ((barrier adj height) (energy adj band) (work adj function)) near2 (asymmetr\$4 d...

L6: (13) 3 and 4

L7: (1813) (257/314,315).CCLS

L8: (212) 3 and 7

L9: (27) 4 and 7

(1) 09/848877

(1813) tunnel adj barrier

(5) low adj (tunnel adj barrier)

(109488) asymmetri\$4

(0) asymmetri\$4 adj (low adj (tunnel adj barrier))

(12792) (float\$3 adj gate) same (control adj gate)

(121) (121) (AP adj gate) same (control adj gate) and (float adj gate)

BrowserQueueClear

ORsUSPAT:US PGPUB: EPO: JPO: DERWENT: IDM: TDB

Default operator: OR

Plurals

Highlight all hit terms initially

4 and 7

Sept 2 003

	U	Inventor *	Document ID	Issue Date	Page	Title	Current OR	Current XRef *	
1	<input type="checkbox"/>	<input type="checkbox"/>	Aozasa, Hiroshi et al.	US 6054734 A	20000425	43	Non-volatile memory cell having dual gate electrodes	257/315	257/314; 257/316;
2	<input type="checkbox"/>	<input type="checkbox"/>	Aozasa, Hiroshi et al.	US 5751037 A	19980512	45	Non-volatile memory cell having dual gate electrodes	257/315	257/317; 257/321;
3	<input type="checkbox"/>	<input type="checkbox"/>	Arase, Kenshiro et al.	US 5614855 A	19980929	15	Nonvolatile memory device and method of manufacturing same	257/315	257/317; 257/322;
4	<input type="checkbox"/>	<input type="checkbox"/>	Blomme, Pieter et al.	US 20020190311 A1	20021219	25	Insulating barrier, NVM bandgap design	257/321	257/314; 257/315;
5	<input type="checkbox"/>	<input type="checkbox"/>	Cuppens, Roger et al.	US 4803402 A	19880729	12	Semiconductor device	365/185.28	257/315; 257/321;
6	<input type="checkbox"/>	<input type="checkbox"/>	Forbes, Leonard	US 20030042528 A1	20030308	28	Sram cells with repressed floating gate memory, low tunnel barrier interpoly insulators	257/315	257/316; 257/E28.128;
7	<input type="checkbox"/>	<input type="checkbox"/>	Forbes, Leonard	US 20020020871 A1	20020221	22	Static NVRAM with ultra thin tunnel oxides	257/315	257/E29.129; 257/E28.304
8	<input type="checkbox"/>	<input type="checkbox"/>	Forbes, Leonard	US 6605961 B1	20030812	24	Low voltage PLA's with ultrathin tunnel oxides	326/41	257/315; 326/101;
9	<input type="checkbox"/>	<input type="checkbox"/>	Forbes, Leonard et al.	US 20030042527 A1	20030308	38	Programmable array logic or memory devices with asymmetrical tunnel barriers	257/315	
10	<input type="checkbox"/>	<input type="checkbox"/>	Forbes, Leonard et al.	US 6437389 B1	20020820	27	Vertical gate transistors in pass transistor programmable logic arrays	257/302	257/314; 257/315;
11	<input type="checkbox"/>	<input type="checkbox"/>	Forbes, Leonard et al.	US 6222788 B1	20010424	28	Vertical gate transistors in pass transistor logic decode circuits	365/230.06	257/302;

Reads

64.88